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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,765	11/07/2001	Franck Roche	00RO30454288	9186

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EXAMINER	
PATEL, NIMESH G	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 09/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,765	ROCHE ET AL.	
	Examiner	Art Unit	
	Nimesh G. Patel	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) [redacted] is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9, 13-19* is/are rejected.

7)☒ Claim(s) 10-12 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20011107*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 10-12 are objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim cannot depend from any other multiple dependent claim. See MPEP § 608.01(n). Accordingly, the claims 10-12 have not been further treated on the merits.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1-9 and 13-19 are rejected under 35 U.S.C. 102(a) as being anticipated by the I2C-Bus Specification, hereinafter referred to as I2C.

4. Regarding claim 1, I2C discloses a method of transmitting data between two devices (D1, MP, D2, PC)(Figure 2), by means of a clock wire (CK)(SCL) and at least one data wire (DT)(SDA), the clock wire being maintained by default on a logic value A(Page 8, Section 5), characterized in that: each device can tie the clock wire to an electric potential representing a logic value B that is the opposite of A; when a datum is transmitted, the two devices tie the clock wire to B (M12, E11, M21, E21)(Page 9, Section 6.2), the device to which the datum is sent does not release the clock wire (CK) while it has not read the datum (M23, E14), the device sending the datum maintains the datum on the data wire (DT) at least until an instant (t3, t4) when the clock wire (CK) is released by the device to which the datum is sent(Page 10, Section 7.1).

5. Regarding claim 2, I2C discloses a method, in which one of the devices is master and the other slave, the master being distinguished from the slave by the fact that it is the first to tie the clock wire to B (M12, M21) when a datum is transmitted, regardless of the direction in which the datum is transmitted(Page 9, Section 6.2).

6. Regarding claim 3, I2C discloses a method, in which, when the master must send a datum to the slave, the master applies the datum to the data wire (M11), then ties the clock wire to B(M12)(Figure 5).

7. Regarding claim 4, I2C discloses a method, in which, when the slave must receive a datum from the master, the slave detects the value B on the clock wire (E10), then ties the clock wire to B(E11) and reads the datum (E12)(Figure 5).

8. Regarding claim 5, I2C discloses a method, in which the time (E13) that the slave has to release the clock wire after receiving a datum, is independent of any action by the master, as the master does not send any new datum while the slave has not released the clock wire (M10, M11)(Page 10, Section 7.1).

9. Regarding claim 6, I2C discloses a method, in which, when the master must receive a datum from the slave, the master ties the clock wire to B (M21)(Figure 5).

10. Regarding claim 7, I2C discloses a method, in which, when the slave must send a datum to the master, the slave detects the value B on the clock wire (E20), then ties the clock wire to B (E21) and applies the datum to the data wire (E22)(Page 7, Section 4).

11. Regarding claim 8, I2C discloses a method, in which the time (E23) that the slave has to release the clock wire after sending a datum, is independent of any action by the master, as the master does not tie the clock wire to B to request sending a new datum while the slave has not released the clock wire (M10)(Page 10, Section 7.1).

12. Regarding claim 9, I2C discloses a method, in which, when the clock wire has the logic value A, the time that the master has to tie the clock wire to B is independent (M16, M24) of any action by the slave(Figure 5).

13. Regarding claim 13, I2C discloses a master-type data transmitting/receiving device (MSTR) comprising a connection terminal to a clock wire (CK)(SCL), at least one connection terminal to a data wire (DT)(SDA), and means for tying the clock wire (CK) to an electric potential B(high) representing a logic value that is the opposite of a logic value A(low), characterized in that it comprises means for performing the following operations, when a datum (B) is to be sent: checking or waiting for the clock wire to have the logic value A (M10)(Page 10, Section 7.1), applying the datum to the data wire (M11), tying the clock wire (M12) to B, then releasing the clock wire (M13), and maintaining the datum on the data wire at least until an instant (t3, t4) when the clock wire has the logic value A (M14, M10)(Figure 6).

14. Regarding claim 14, I2C discloses, further comprising means for performing the following operations, when a datum is to be received: checking or waiting for the clock wire to have the logic value A (M20), tying the clock wire (M21) to B, reading the datum on the data wire (M22), then releasing the clock wire (M23)(Figure 6).

15. Regarding claim 15, I2C discloses Slave-type data transmitting/receiving device (SLV, SLV+HWC) intended to communicate with a master-type device (MSTR) according to one of claims 13 and 14, comprising a connection terminal (CKP) to a clock wire (CK)(SCL), at least one connection terminal (CDT) to a data wire (DT)(SDA), and means for tying the clock wire to an electric potential B(Page 10, Section 7.1) representing a logic value that is the opposite of a logic value A, characterized in that it comprises means for performing the following operations, when a datum (B) is to be received: detecting a change from A to B on the clock wire (E10),

tying the clock wire (E11) to B, reading the datum on the data wire (E12), and releasing the clock wire (E14)(Figure 6).

16. Regarding claim 16, I2C discloses, further comprising means for performing the following operations, when a datum is to be sent: detecting a change from A to B on the clock wire (E20), tying the clock wire (E21) to B, applying the datum to the data wire (E22), and releasing the clock wire (E24)(Page 7, Section 4).

17. Regarding claim 17, I2C discloses a synchronous data transmission system, characterized in that it comprises a master-type device (MSTR) according to one of claims 13 and 14 linked by a clock wire (CK) and at least one data wire (DT) to a slave-type device (SLV) according to one of claims 15 and 16(Figure 6).

18. Regarding claim 18, I2C discloses a slave-type communication interface circuit (HWC) linked or intended to be linked by means of a clock wire (CK) and at least one data wire (DT) to a master-type device (MSTR) according to one of claims 13 and 14, characterized in that it comprises: means for tying the clock wire to an electric potential B representing a logic value that is the opposite of a logic value A, trigger means (FD1, FD2) to automatically tie the clock wire to B when the clock wire changes from A to B(Page 10, Section 7.1), an input (ACK) to apply a clock wire release signal to the trigger means, and an output to deliver an information signal (STATUS) that has a first value when the clock wire is tied to B by the trigger means and a second value when the clock wire is released by the trigger means(Page 10, Section 7.2).

19. Regarding claim 19, I2C discloses a communication interface circuit, further comprising: means (FD4) for storing at least one datum, and means (FD3, FD4) for automatically applying the datum to the data wire when the clock wire changes from A to B(Figure 3).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nimesh G. Patel whose telephone number is 571-272-3640. The examiner can normally be reached on M-F, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nimesh G Patel
Examiner
Art Unit 2112

NP
September 9, 2005

TIM VO
PRIMARY EXAMINER